



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,670	01/26/2004	Jean-Yves Simon	TI-36989	9476

23494	7590	02/22/2008
TEXAS INSTRUMENTS INCORPORATED		
P O BOX 655474, M/S 3999		
DALLAS, TX 75265		

EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2112	

NOTIFICATION DATE	DELIVERY MODE
02/22/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com  
uspto@dlemail.itg.ti.com

**Office Action Summary**

Application No.

10/764,670

Applicant(s)

SIMON, JEAN-YVES

Examiner

Fritz Alphonse

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 December 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This Office Action is in response to the Request for Continued Examination (RCE) filed on 12/17/2007. Claims 1-26 are pending.

#### ***Continued Examination Under 37 CFR 1.114***

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/17/2007 has been entered.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6-10, 18-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston (U.S. Pat. No. 6,906,961) in view of Wei (U. S. Pat. No. 6,683,817) and further in view of Ito (US. Pub. 2004/0221098 A1).

As to claim 6, Eggleston (figs. 1-3) shows a system (134), including a flash memory (100); a controller (130) coupled to the flash memory (100); and at least one register (128/114) coupled to the controller (130).

Eggleston differs from claim 6 in that he does not explicitly disclose “a controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block.”

However, the limitation is obvious and well known in the art, as evidenced by Wei (See figure 2a; col. 5, lines 58 through col. 6 line 14). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to incorporate Eggleston’s flash memory device into the electronic circuit, as disclosed by Wei. Doing so would provide improved data transfer for the NAND Flash memory and which can furthermore assure data integrity (col. 2, lines 5-8).

In addition, as to claim 6, Eggleston does not explicitly disclose a switch coupled to a controller and a system that stores the ECC in a plurality of registers using a switch. However, the limitations are obvious and well known in the art, as evidenced by Ito (see fig. 6; paragraph 0143).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to improve upon the semiconductor integrated circuit device, as disclosed by Ito. Doing so would provide an IC circuit comprising an ECC controller for controlling and ECC circuit under control of a control logic.

As to claims 7-10, Eggleston discloses a system, wherein the flash memory is a NAND Flash memory (col. 5, lines 40-49); the system stores a first portion of the ECC in a first register; and storing a second portion of the ECC in an alternate register if the first register is full (fig. 8; col. 16, lines 45 through col. 17 line 5). Eggleston discloses a system, wherein the controller transfers contents of all registers to memory (col. 16, lines 9-30).

As to claim 1, method claim 1 corresponds to apparatus claim 6; therefore, it is analyzed as previously discussed in claim 6 above.

As to claims 2-4, Eggleston (fig. 8 A-B) discloses a method, comprising: storing a first portion of the ECC in a first register; and storing a second portion of the ECC in a second register if the first register is full (col. 16, lines 31-66).

As to claims 18-19, the claims have substantially the limitations of claims 6 and 10; therefore, they are analyzed as previously discussed in claims 6 and 10 above.

As to claims 20-23 Eggleston discloses a system, wherein the flash memory is a NAND Flash memory (col. 5, lines 40-49); the means for selectively storing the ECC is configured to stores a first portion of the ECC in a first register; and storing a second portion of the ECC in an alternate register if the first register is full (fig. 8; col. 16, lines 45 through col. 17 line 5). Eggleston discloses a system, wherein the controller transfers contents of all registers to memory (col. 16, lines 9-30).

As to claims 24-26, Eggleston discloses a system, wherein the registers (224-228) are in the controllers.

4. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston (U.S. Pat. No. 6,906,961) in view of Kikuchi (U. S. Pat. No. 6,131,139).

As to claim 12, Eggleston discloses a system comprising: a means for storing a data block (i.e., flash memory 100); a means for transferring a data block (i.e., controller 130).

Eggleston does not explicitly teach means for simultaneously computing an ECC of the data block; means for shifting the data block between the means for storing and means for controlling while computing an ECC for said data block.

Art Unit: 2112

However, the limitation is obvious and very well known in the art, as evidenced by Kikuchi (figs. 2, 11, col. 16, lines 30-41).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to improve upon the memory device, as disclosed by Kikuchi. Doing so would provide a split data error correction code circuit to generate an ECC code from user data.

As to claims 13-16, Eggleston discloses a system, wherein the flash memory is a NAND Flash memory (col. 5, lines 40-49); the means for selectively storing the ECC is configured to store a first portion of the ECC in a first register; and storing a second portion of the ECC in an alternate register if the first register is full (fig. 8; col. 16, lines 45 through col. 17 line 5). Eggleston discloses a system, wherein the controller transfers contents of all registers to memory (col. 16, lines 9-30).

5. Claims 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston in view of Kikuchi and Ito as applied to claims 1, 6, and further in view of Acton (U.S. Pat. No. 6,594,792).

As to claims 5, 11, Eggleston and Kikuchi do not disclose a system, wherein the controller is configured to compute the ECC while performing the Exclusive-OR function. However, the limitation is obvious and well known in the art, as evidenced by Acton (col. 7, lines 30-47).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to improve upon the data processing system, as disclosed by Acton. By doing so, a different error correction code may be used which provides double-bit or greater error correction capability.

Art Unit: 2112

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston in view of Kikuchi and Ito as applied to claim 12, and further in view of Acton (U.S. Pat. No. 6,594,792).

***Response to Arguments***

7. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

**or faxed to:** (703) 872-9306 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished


Art Unit: 2112

applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Fritz Alphonse

Art Unit 2112

February 14, 2008

  
JACQUES LOUIS JACQUES  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100